Daniel A. Staver

dan.staver@tavetech.com (719) 359-5352 Skype: tavetech
Tave Tech Corporation 3130 Hollycrest Dr., Colorado Springs, CO 80920 www.tavetech.com

Objective: Product development of DSP-based metrology and RF communications products.

Available for consulting/part-time: engineering, hardware or firmware,
computer script generation for efficient data processing (either repetitive or one-off),
remote project management.

Education:

M.Eng. EE	Cornell University, 1984
BS EE	Cornell University, 1982

Specific Skills:

- Project leadership in design of complex systems and products using digital & mixed analog-digital integrated circuits, custom ASICs, COTS† devices and innovative DSP algorithms. († Commercial-Off-The-Shelf)
- Thirty plus years industrial experience in digital & mixed signal analog-digital system design: printed circuit board and system design & test; metrology system and DSP design, embedded system programming, instrumentation & sensor interfacing for a broad base of industrial, medical, consumer and government applications and products.
- Integrated Circuit design and project management of digital & mixed-signal analog-digital IC's and UHF RFID IC's.
- Extensive embedded code development in C using: TI DSP/MSP430 family, SiLabs 32-bit ARM, Atmel ARM SAM families, MicroChip uControllers, 8048 family, TI/Chipcon CC1xxx family, Bluegiga WF121 WiFi module, Telit GPS modules.
- Extensive experience with electricity metering applications, DSP metrology, and metering platforms: Atmel SAM4CMx, Microchip PIC32CXMTx, and ATM90Exx families.
- Authored best-in-class DSP-based metrology for wide-bandwidth electricity metering.
- Innovative application of DSP (Digital Signal Processing) to products and systems, custom DSP-course design.
- Custom data filtering and script development, developed secure automated web-based data filtering service using PHP/MySQL.
- Primary customer contact: work with customers to learn their application, define system goals, and, by determining what is needed *vs.* what is initially wanted, develop a more optimal system solution.
- Experience in managing projects with varied, cross-cultural and remote resources. I have managed projects with concurrent resources in the U.S., Switzerland, the Czech Republic and Slovenia.
- Experience in communicating cross culturally: Mandarin Chinese - spoken, German - written and spoken, French: written & spoken (learning). I have quite a bit of cross-cultural experience and can speak Mandarin Chinese, some French, German, Spanish and Czech and I know a few words/phrases in many languages just for fun. It's good to be able to "break the ice" in just about any situation.
- Tools experience, simulation & modeling: Matlab/Octave, IDL, Saber, SPICE, experience developing FPGA-based systems using VHDL & Verilog for both Altera and Xilinx targets, Python, awk, C/C++, Fortran, Pascal, Forth, Excel, Cadence, various CAD tools, RF experience to 2.5GHz, programming various uC families, as well as others. Computing environments: UNIX tools & filters, Windows, DEC.
- Six Sigma Green Belt Certified. I try to be educable.
- 38 US Patents granted.

Experience:

(3/2008 - Present) President, Tave Tech Corporation, Colorado Springs, CO:

- Developing world-class customizable metrology products for use on any MCU platform, avoiding pitfalls of being tied to a specific MCU platform, offering freedom in times of sourcing uncertainty.
- Developing RF communications products.
- Developed best-in-the-world DSP-based metrology embedded code for Microchip/Atmel's line of metrology ASICs (PIC32CXMTx, SAM4CMx). Worked with team to develop and market dual-core 32-bit ARM metering product line.
- Developed embedded coding for smart battery which has since sold > $25M.
- Developed very high-sensitivity 915MHz DSSS (Direct Sequence Spread Spectrum) radio system, with GPS and built-in WiFi server.
- Currently in initial product development phase of RF communication consumer products including security and entertainment applications.
- Developed an ISM-band (915MHz) RF Interference Testbed for RFID IC compliance testing using Python to automate and expedite user operation for extensive device testing.
- Electrical engineering consulting services and embedded system development.

(1/2017 – 12/2022) Staff Applications Engineer, Microchip Technology Inc., Colorado Springs, CO:

- Develop next generation best-in-the-world DSP-based metrology embedded code for Microchip/Atmel's line of metrology PIC SOCs.
- Support metrology customers world-wide with sales, trouble shooting, and metrology customization.

(9/2001 – 5/2008) US-ASICs Group Leader, EM Microelectronic-US, Colorado Springs, CO:

- Matrix management of mixed-signal design group, new project evaluation and estimation, customer interface, spec negotiation, progress tracking, negotiating resource allocation, technical contribution in analysis, digital design, RF measurement & analysis.
    - Project manager and customer contact for various low-voltage/low-power ASIC's, RFID chips, encryption & authentication, dispersed team: US, Switzerland, Czech Republic, Germany and Slovenia.
    - Get IC's into production and keep them in production, keep the customer happy, creative problem solving, keep the fab happy, production planning, lab tests, modeling and analysis to support product development, qualification and production involving low-freq general instrumentation & measurement as well as RF measurement to 2.5GHz.

(7/1984 – 9/2001) Senior Staff, GE Corporate Research and Development Center, Schenectady, NY:

- Lead teams of designers and layout technicians in developing mixed-signal analog-digital ASICs and systems for industrial, medical and government applications.

Various system design projects:

- Detector Framing Node (DFN) - Complex full-size PCI board which interfaces solid-state X-ray detector electronics via 1.25GHz optical Fibre Channel link to PC. Responsible for all aspects of hardware design and architecture, component selection, supervision of board layout (12-layer board), population and support during production. Board fully functioned first pass.

- Aux. Image Interface (AIMI) Board – Complex daughter card for DFN board allows alternate real-time image processing, responsible for all aspects of board design.
- Data Acquisition Platform Project – Project leader responsible for: directed customer in defining system partitioning and specs; definition of meter/ASIC partitioning; overall system design of mixed-signal analog-digital ASIC; design of control logic, digital decimation filter, and sensor drive architecture. ASIC worked in customer's kV Meter application first-silicon.
- Developed DSP-based metering algorithms for the GE kV& kV^2 Meter product lines.
  Authored and taught DSP course "DSP for Metering Applications" at request of internal GE component. Traveled off-site to teach 6-day course over a 3-wk period to approximately 17 engineers who then with my guidance implemented my filtering architecture in the GE kV and kV^2 meter product lines.
- High-Speed Modem Project - Responsible for all aspects of project design and development and source selection of modem protocol IP. Delivered working DSP-based modem board (first pass) capable of performing desired V.32-bis protocol and embedded functions, as well as up to V.90 protocol; in-field re-programmable - at a 30% lower cost than current V.22-bis modem and at 65% lower cost than customer's expected development approach.
- Jet Engine Turbine Tip Clearance Measurement Project - Researched and invented a new approach for high accuracy high temperature turbine tip-clearance measurement system.

Various digital ASICs and/or ASIC-based systems designs:

- Coordinate stabilization project - project leader and designer: responsible for system definition, algorithm implementation for two ASICs developed simultaneously - both worked in application first-pass silicon.
- First in the world single-chip multiply & accumulate double-precision (64-bit) / single-precision (32-bit) floating point / 32-bit integer - numeric 40MHz co-processor - responsible for design of exponent data path, arithmetic control, top-level block placement and floor-planning. Successfully fab'ed, tested and worked in demonstration system.
- Single-precision 30 MFLOPS floating point multiply/accumulate chip - responsible for design of exponent data path, control, and test. Successfully inserted into product (GE Graphicon graphics engine). My first chip designed in industry and I learned from many mistakes, both mine and others'. Finally worked after a few passes.

(1982 - 1983) Chung-Yuan Christain University, Chung-Li, Taiwan, ROC: Research Assistant - EE Dept.

- Assisted in design of 4-patient arrhythmia monitoring / cardiac disease diagnostic system. I was responsible for: processor configuration, output data processing / presentation, and built-in-test. After I left Taiwan, the team doubled the memory to make an 8-patient system and fielded units for use in many Taiwan National Hospitals' Intensive Care Units.
- Lectured cross-culturally on various topics in EE / CS as a substitute lecturer.

(1980 - 1981) Cornell University, Ithaca, NY, Dept. of EE: Experimental Electric Car Project Member

- Researched lead-acid storage cells, fast charging systems. Drove & maintained vehicle and repaired vehicle's drive electronics as needed, especially after when the field drive transistors blew and the armature current pegged the ammeter at 2000A. It was an exciting time to be driving.

  This generation of Cornell's Experimental Electric vehicle was powered by a GE 25HP DC shunt-wound field-control motor running off an 84V battery pack built into a replica 1931 Alpha-Romeo red roadster body (very cool).

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I have 38 US patents granted with additional patents pending, not including foreign patent filings.

Patents granted:

#11,460,492, Electrical energy loss detection, Staver, 10/4/2022.

#11,415,606, Systems and methods for improved root mean square (RMS) measurement, Staver, 08/16/22

#10,914,770, Electrical energy loss detection, Staver, 2/9/2021.

#10,809,284, Systems and methods for improved root mean square (RMS) measurement, Staver, 10/20/20

#8,319,509, Testing circuit for an analog to digital converter, Staver, Kazazian, 4/30/12

#7,548,223, Reduced cost automatic meter reading system and method using locally communicating utility meters, Brooksby, Harrison, Staver, Berkcan, Hoctor, Daum, Welles, 6/16/09

#7,269,239, Simple two-wire communication protocol with feedback status, Staver, Wall, Tran, 9/11/07

#6,970,586, Detector framing node architecture to communicate image data, Baertsch, Dixon, Staver, Van Stralen, Wodnicki, 11/29/05

#6,904,124, Indirect programming of detector framing node, Staver, Van Stralen, Wodnicki, 6/7/05

#6,901,159, Communication of image data from image detector to host computer, Baertsch, Dixon, Staver, Van Stralen, Wodnicki, 5/31/05

#6,816,360, Reduced cost automatic meter reading system and method using locally communicating utility meters, Brooksby, Harrison, Staver, Berkcan, Hoctor, Daum, Welles, 11/9/04

#6,738,934, On-chip watchdog circuit, Frank, Staver, 5/18/04

#6,681,011, Method and modem circuit using a dither signal for determining connection status of a phone line, Staver, Brooksby, 1/20/04

#6,675,463, Methods for forming toroidal windings for current sensors, Berkcan, Staver, Daum, Elmore, 5/13/04

#6,487,625, Circuit and method for achieving hold time compatibility between data-source devices coupled to a data-requesting device through a data bus, Staver, Frank, 11/26/02

#6,470,071, Real time data acquisition system including decoupled host computer, Baertsch, Dixon, Staver, Van Stralen, Wodnicki, Tkaczyk, 10/22/02

#6,462,673, Asymmetric-rate communication method and system for remote data collection, Brooksby, Staver, 10/22/02

#6,400,130, Primary current conductor configurations for a residential electronic, Berkcan, Staver, Elmore, Coburn, Watts, 6/04/02

#6,393,123, Method and modem circuit for determining connection status of a phone line, Staver, Frank, 5/21/02

#6,262,672, Reduced cost automatic meter reading system and method using locally communicating utility meters, Brooksby, Harrison, Staver, Berkcan, Hoctor, Daum, Welles, 7/17/01

#6,242,922, Arc detection architecture based on correlation for circuit breakers, Daum, Staver, 6/5/01

#6,173,236, Vector electricity meters and associated vector electricity metering methods, Elmore, Staver, 1/9/01.

#5,978,741, Vacuum Fixture, (naming error on USPTO side, but we like the name so we'd like to keep it :-) Elmore, Staver, Mammen, 11/2/99 (this concerns signal filtering and reactive power metering)

#5,677,845, Programmable data acquisition system for collecting electrical power signals, Staver, Ho, McGrath, 10/14/97

#5,673,196, Vector electricity meters and associated vector electricity metering methods, Hoffman, Provost, Maehl, Lavoie, Plis, Elmore, Germer, Mammen, Bullock, Putcha, Staver, Burt, Crittenden, Edge, 09/30/97

#5,650,951, Programmable data acquisition system with a microprocessor for correcting magnitude and phase of quantized signals while providing a substantially linear phase response, Staver, 07/22/97

#5,589,766, Field-testable integrated circuit and method of testing, Frank, McGrath, Staver, 12/31/96

#5,568,047, Current sensor and method using differentially generated feedback, Staver, Hakkarainen, 10/22/96

#5,548,540, Decimation filter having a selectable decimation ratio, Staver, McGrath, 8/20/96

#5,463,569, Decimation filter using a zero-fill circuit for providing a selectable decimation ratio, Staver, McGrath, 10/31/95

#5,436,858, Decimation circuit and method for filtering quantized signals while providing phase angle correction with a substantially linear phase response, Staver, 07/25/95

#5,410,498, Decimation circuit and method for filtering quantized signals while providing a substantially uniform magnitude and a substantially linear phase response, Staver, 04/25/95

#5,142,488, Serial memories operated for re-ordering samples, Chan, Staver, 8/25/92

#5,111,421, System for performing addition and subtraction of signed magnitude floating point binary numbers, Molnar, Ho, Staver, Molnar, 5/5/92

#5,021,987, Chain-serial matrix multipliers, Chan, Staver, 6/4/91

#5,001,647, Inertial transformation matrix generator, Rapiejko, Chan, Staver, Clark, 3/19/91; EPO - #90309350.8-

#4,901,263, Versatile data shifter with sticky bit generation capability, Ho, Molnar, Staver, 2/13/90

#4,841,467, Architecture to implement floating point multiply/accumulate operations, Ho, Molnar, Staver, 6/20/89

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Publications:

Internal GE Publication, Mar. 1992, D. Staver

``Spatial Processing Techniques for the Detection of Small Targets in IR Clutter'', SPIE Tech. Sym. on OE/Aerospace Sensing, April 1990, D.S.K. Chan, D. Langan, D. Staver

``A 40MHz 64-bit Floating Point Coprocessor'', IEEE ISSCC, 1989, K. Molnar, C.Y. Ho, D. Staver, B. Davis, R. Jerdonek

``A 30 MFLOPS CMOS Single Precision Floating Point Multiply/Accumulate Chip'', IEEE ISSCC, 1987, D. Staver, C.Y. Ho, K. Molnar, R. Baertsch

``A High Performance 1.25 Micron CMOS Floating Point Multiply/Accumulate Chip'', IEEE CICC, 1985, C.Y. Ho, R. Jerdonek, K. Molnar, D. Staver

``A High Performance 1.25 Micron CMOS Floating Point Multiply/Accumulate Chip'', GOSAM Symposium, May 1985, C.Y. Ho, R. Jerdonek, K. Molnar, D. Staver

``Harmonics of Harmonicas'' ELECTRO-NOTES, Special Edition ``E'', Vol 15, No. 161-163, May `84 - July `84, D. Staver

``Single Chip Microcomputer Implementation of Home Bus Compatible Devices'', GOSAM Microprocessor Symposium, October 1981, D. Staver, R. Fearing, M. Barton

References on request.

DFN board: Interface board to GE's Apollo Solid-state X-ray imager

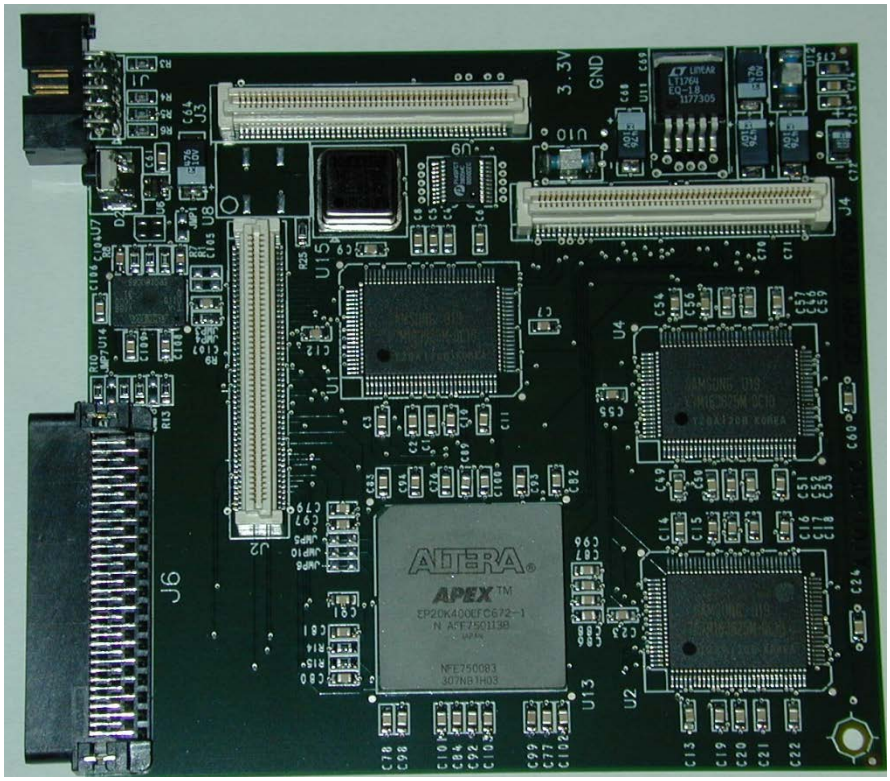
Responsible for all hardware design, planning of part placement, FPGA pin/net assignment to minimize routing bottlenecks, board manufacturing interface and transition to production.

Developed novel technique for pre-planning the flow of thousands of nets and pin selection for large pin FPGA board designs to ease net auto-routing. Full-size PCI card (12-layer board) interfaces to solid-state X-ray imagining panel via 1.25GHz Fibre-channel.

Single PC with DFN card & driver replaced SPARC station, microprocessor board with custom high-end DSP daughter-board, and PC.

Board worked first pass out of fab with the only problem being the polarity had been reversed on one electrolytic cap footprint. Lesson is that even the easy parts can cause problems and not to take any part footprint for granted.

AIMI daughter-board: Provides platform to reformat data from standard SE Apollo X-ray imager into an alternate image processing system's native format (attaches to test connectors of DFN board).

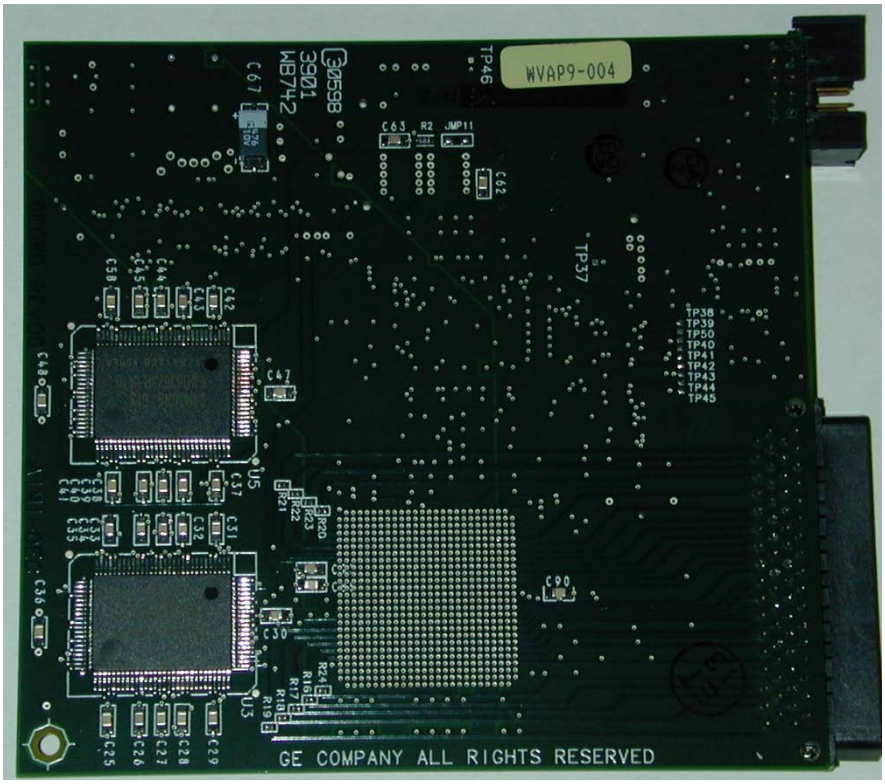


Responsible for all hardware design, planning of part placement, FPGA pin/net assignment to minimize routing bottlenecks as well as original idea for interrupting normal data flow of DFN card allowing AIMI card to “sniff” for frame transfer and gracefully grab the data, reformat as needed and pass on to its output image processing chain without special application firmware needed for DFN except a minor change to the standard DFN firmware image release.

Allows interface between standard solid-state X-ray imaging system via standard release DFN card and special output image processing via other imaging post processing and display systems.

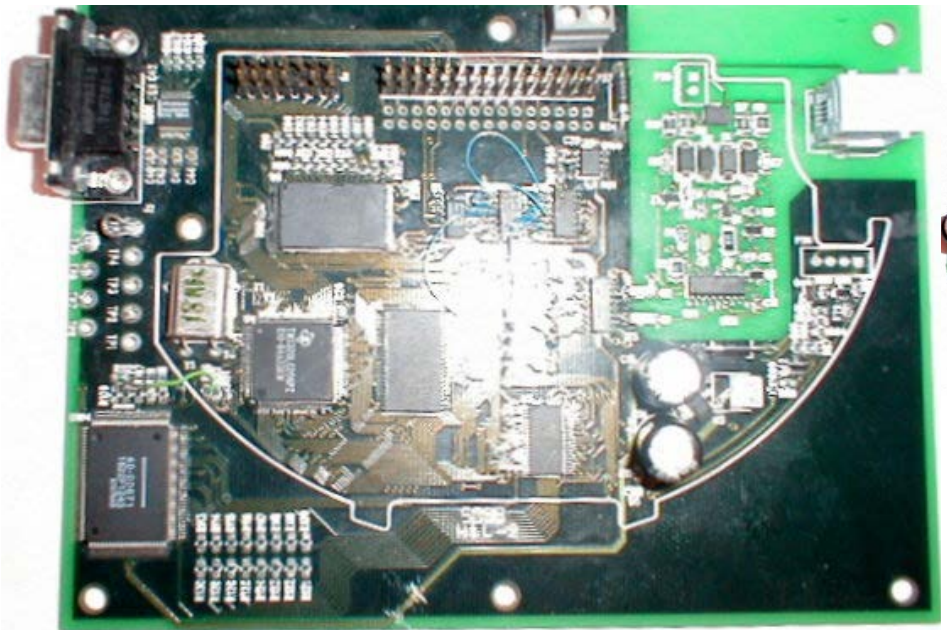
Board worked after change in control pin polarity for programming loop of FPGA due to a mistake in the FPGA initial manufacturer's documentation.

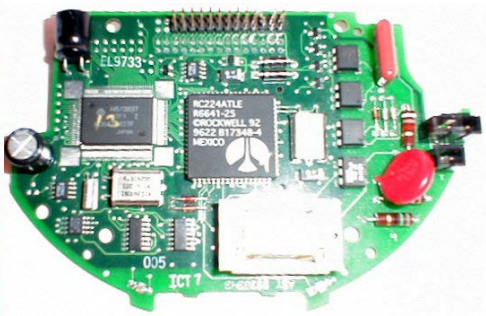
Lesson: stay away from new parts, but if cannot be avoided, then correlate pin syntax with older family parts to see if anything appears to have changed.



Various Metering applications development:

Low-cost residential meter platform (upper right) – responsible for board design, sensor interface, DSP architecture and DSP filtering.
First turn achieved very good performance (flatness & accuracy) over wide current range. (current sensor not shown)





Low-cost V.32bis (14.4K) meter phone modem (lower-left). Responsible for architecture, design, layout and signal processing integration of external modem IP.
Demonstrated functional field-upgradeable DSP-based platform (lower-left) capable of up to V.90 (56K) modem at less cost than existing v.22bis (2.4K) socket-modem chipset-based solution (lower-right).

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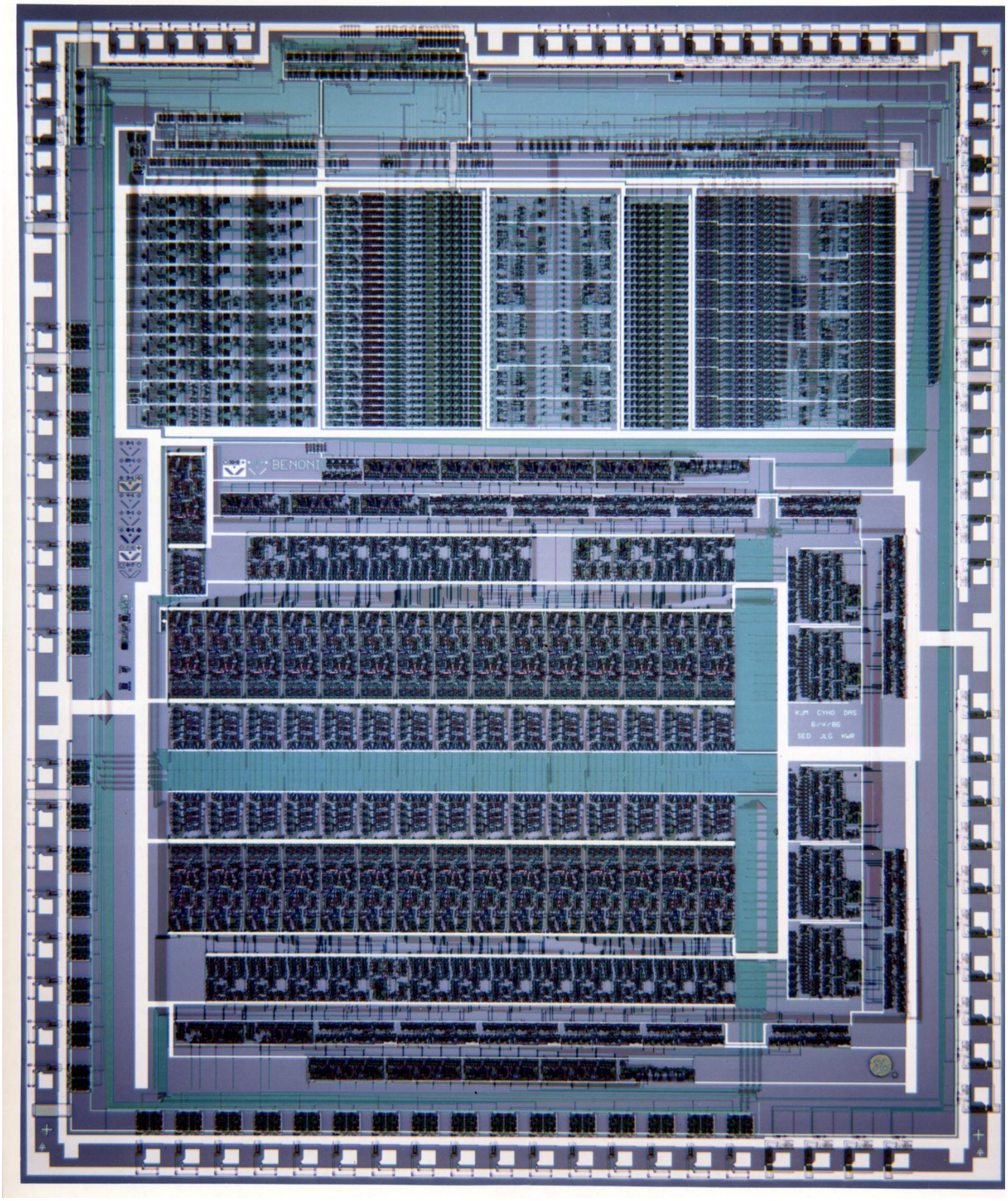
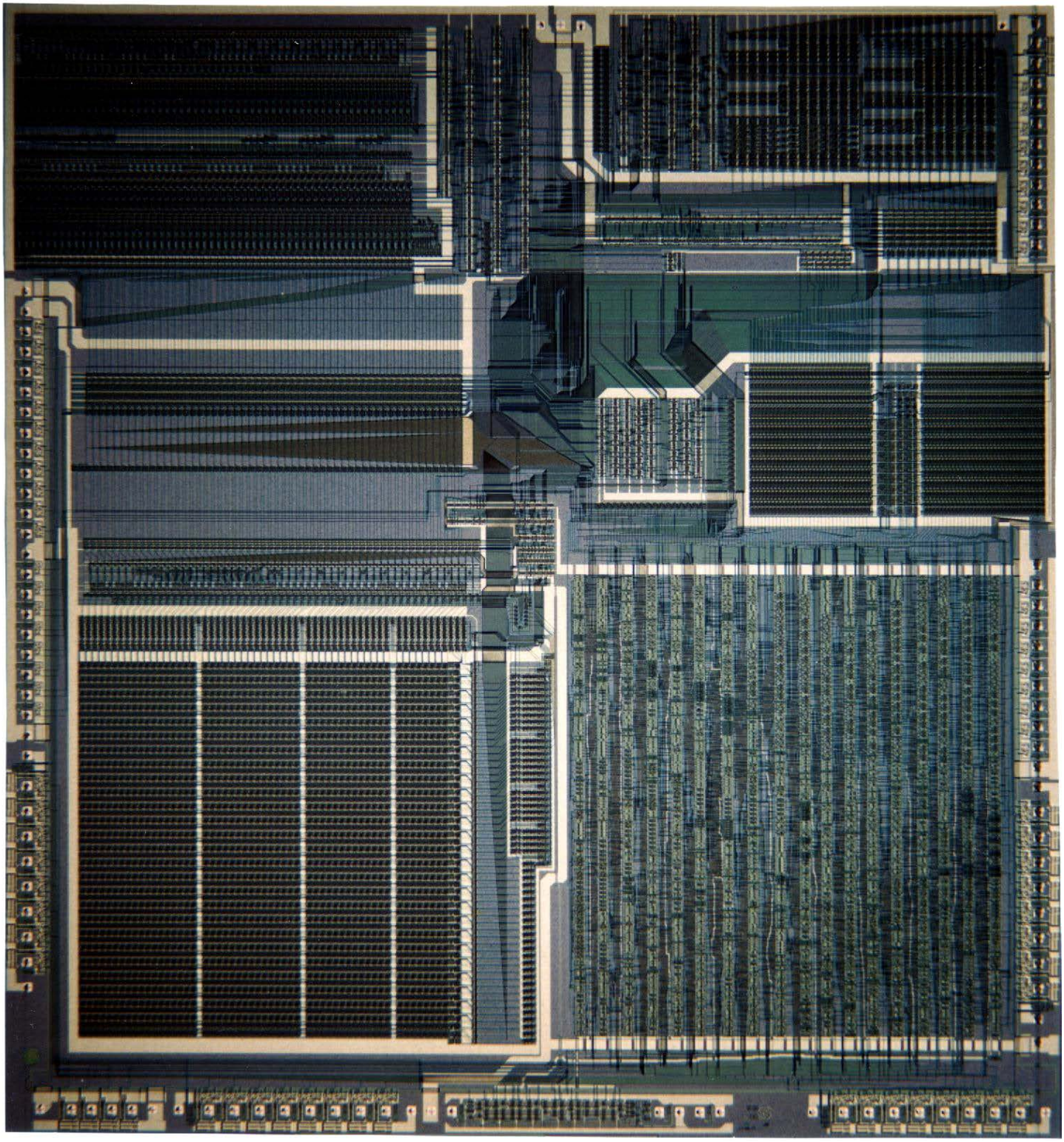
Benoni – Multiply/Accumulate Chip
30MHz Single Precision Multiply/Accumulate Chip
CMOS; 1.2µ/1.4µ (drawn), 1.0µ/1.0µ (effective); Die size: 7.2 x 8.0 mm (280 x 315 mils); 56K transistors

Responsible for design of exponent data path, overall logic control & implementation, and test.



Baby Bear - RPM-40
40MHz 64-Bit Floating-Point Co-Processor
Single Precision Floating-Point (32-bit)/ Double Precision Floating-Point (64-bit), 32-bit Integer Numeric Co-Processor
CMOS; 1.2µ (drawn); Die size: 11.2 x 10.4 mm (440 x 410 mils); 170K transistors

Responsible for design of exponent data path, arithmetic control logic, top-level block placement and die floor-planning. Successfully fab'ed, tested and worked in demonstration system.



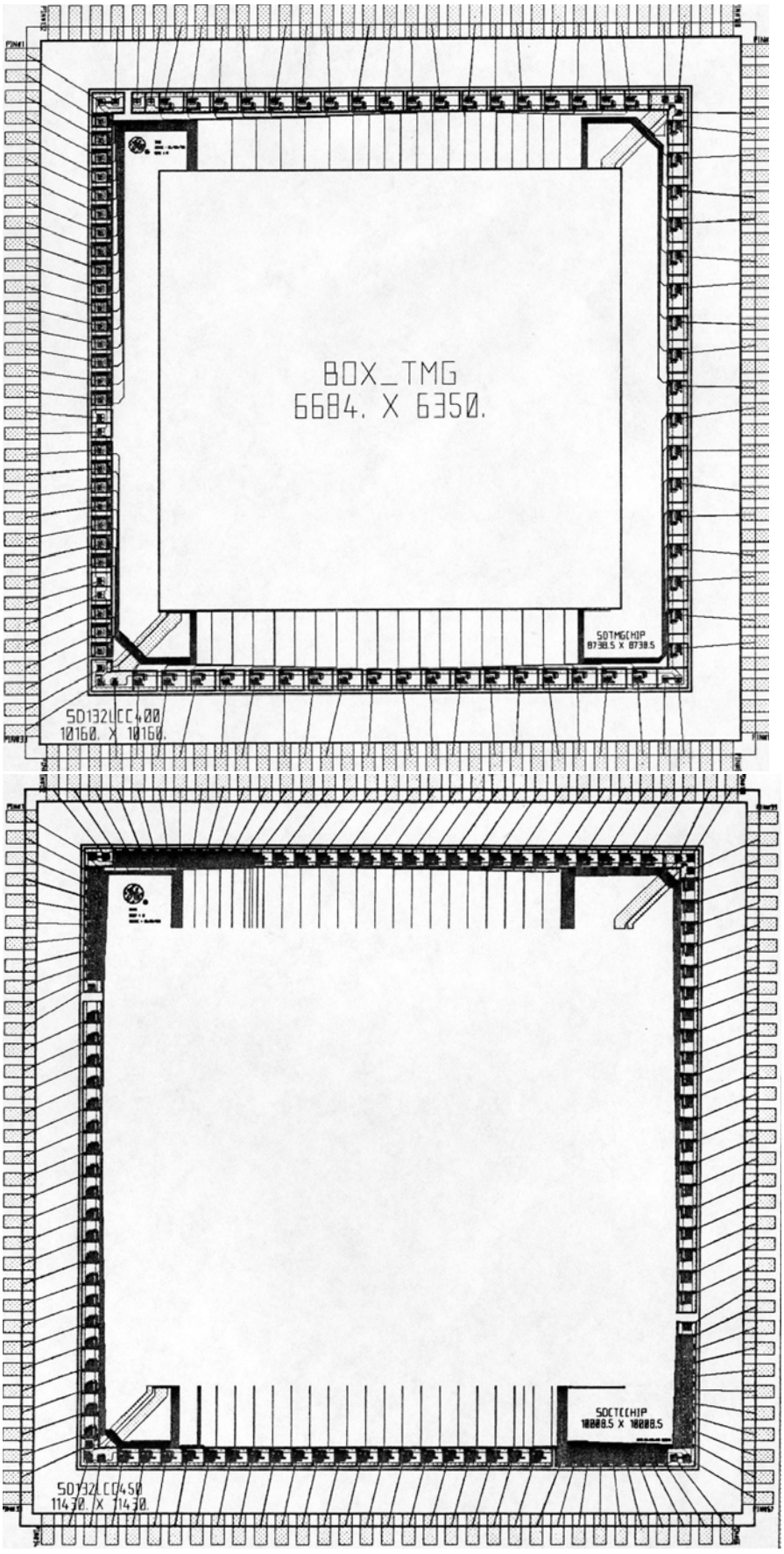
TMG Chip (top)
Transform Matrix Generator Chip
CMOS; Die size: 8.7 x 8.7 mm
(345 x 345 mils)

The TMG chip continuously generated stabilization matrices for sensor data using a set of co-located rate integrating gyros.

CTC ASIC (bottom)
Coordinate Transform Chip
CMOS; Die size: 10.0 x 10.0 mm
(395 x 395 mils)

The CTC chip continuously transformed non-inertial data from multiple sensors into a stabilized inertial coordinate space for subsequent data processing.

Project Leader: Worked with team and customer to develop system spec. Responsible for sub-system definition, algorithm optimization and ASIC implementation using a newly developed in-house bit-serial arithmetic silicon compiler language/tool for simultaneous development of two ASICs (TMG & CTC), pad definition and layout supervision for very fast turn-around, fault simulation and test.
Both ASICs worked in application using first-pass silicon.



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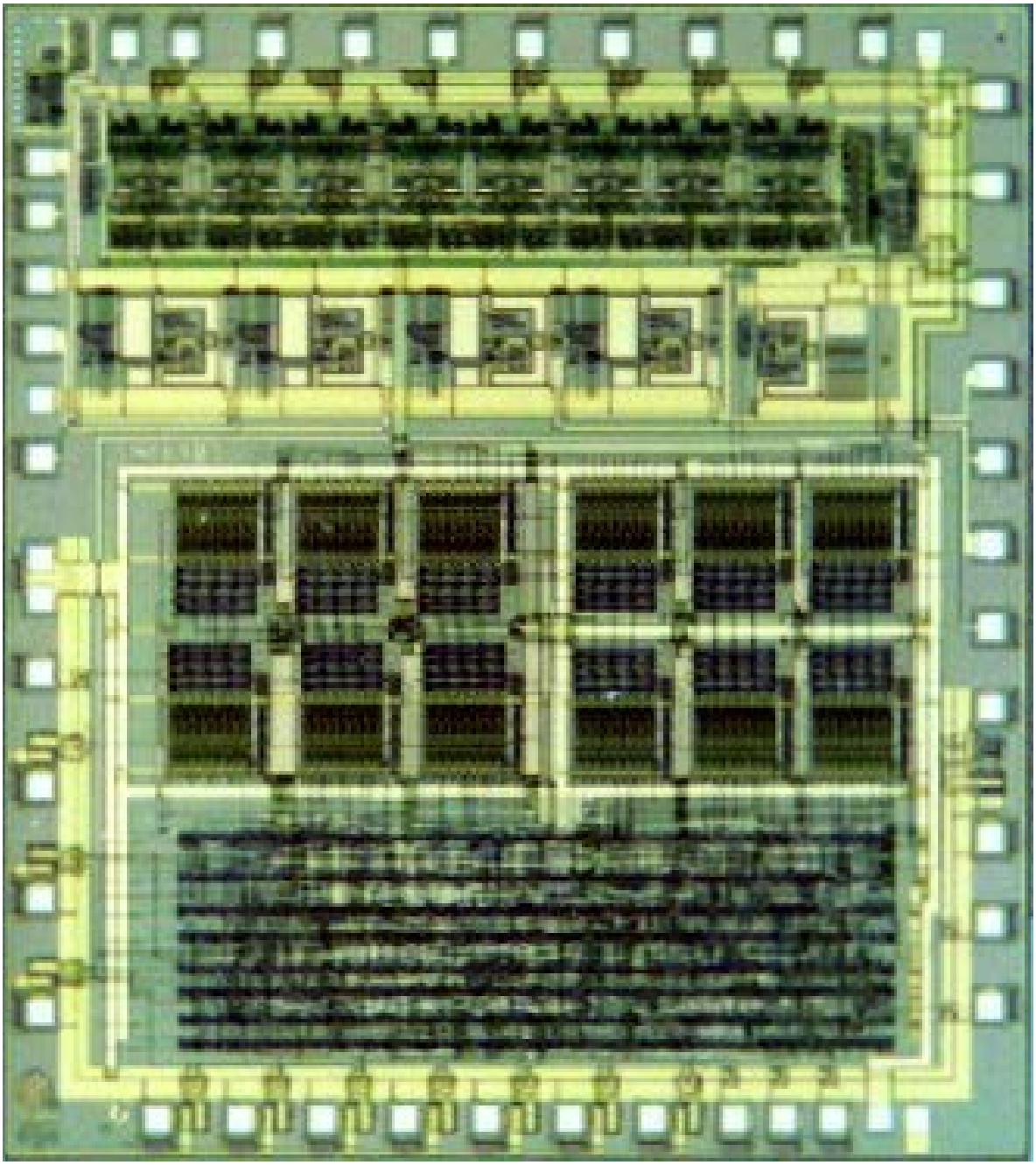
Tekel – DAP Chip
10MHz Programmable Data Acquisition Platform
8-Channel Δ/Σ A/D, 4-Channel Zero-Flux Current Sensor Interface
CMOS; 1.0µ (drawn); Die size: 5.1 x 5.1 mm (200 x 200 mils)

Project Leader: Directed customer in definition of overall meter system architecture, system/ASIC partitioning and specs; Responsible for overall system design of mixed-signal analog-digital ASIC, designed control, on-chip variable digital decimation filter, and sensor drive architecture, fault simulation and test; qualification and getting ASIC into production; customer support; Designed entire subsequent downstream DSP filtering chain for line of electricity meters; Authored and taught an accompanying DSP course to my customer's engineers for implementation of DSP chain. ASIC worked in customer's *kV Meter* application first-silicon and in production for ~20 years and millions of *kV*-class meters.



UHF RFID Chip
Very-low power beam-powered UHF RFID ASIC with encryption engine for secure transaction processing via mutual authentication.
CMOS; 0.5µ

Project Leader - Responsible for: overall project execution using cross-cultural concurrent design resources in Slovenia, Czech Republic, Switzerland, and the U.S; implementation of digital encryption engine, supervision of analog design and integration, design and implementation of a custom fault-simulation tool due to special nature of design and fault grading, qualification of chip and production maintenance and design changes to accommodate process changes to maintain strict impedance control for high-Q 915MHz operation. Assisted customer with RF design of impedance matching for flip-chip mounting option.